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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,246	11/02/2001	John R. Nickolls	42113/CAG/B600	2122

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,246	NICKOLLS ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/27/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-34,36 and 84-97* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *84-97* is/are allowed.

6)☒ Claim(s) *14,15,17-34 and 36* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/6/02 5/9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 14-34, 36, and 84-97 in the reply filed on 9/27/04 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 14, 15, 17-34, and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Trimberger (U.S. Patent No. 6,023,564) (hereafter referred to as Trimberger'564).

Referring to claim 14, Trimberger'564 discloses, as claimed, a method of controlling a reconfigurable processor (see Fig. 1), comprising: executing a first instruction (the instruction for initialize the values in configuration registers

(101a-101n, see Fig. 1), see Col. 6, lines 47-50, regarding the instructions for the selected configuration word being stored in the configuration store 101) that loads a configuration (CONFIG WORD 0-n, see Fig. 1) into a configuration register (101a-101n, see Fig. 1); executing a second instruction (113, see Fig. 1) that references (by CONFIG(X) 124, see Fig. 1) the configuration register; and executing the configuration (CONFIG WORD 0-n, see Fig. 1) in the configuration register (101a-101n registers, see Fig. 1) referenced by the second instruction (113, see Fig. 1).

As to claim 15, Trimberger'564 also discloses: executing the first instruction loads a plurality of configurations into respective configuration registers (see Col. 6, lines 47-50, regarding the instructions for the selected configuration word being stored in the configuration store 101), wherein one of the plurality of configurations (CONFIG WORD 0-n, see Fig. 1) is loaded into a configuration register (one of the 101a-101n registers, see Fig. 1).

As to claim 17, Trimberger'564 also discloses: an application program (inside instruction memory 110, see Fig. 1) issues the first instruction (the instruction for initialize the values in configuration registers (101a-101n, see Fig. 1), see Col. 6, lines 47-50, regarding the instructions for the selected configuration word being stored in the configuration store 101).

As to claim 18, Trimberger'564 also discloses: a compiler generates the first instruction (the instruction for initialize the values in configuration registers (101a-101n, see Fig. 1), see Col. 6, lines 47-50, regarding the instructions for the selected configuration word being stored in the configuration store 101). Note as in a regular system, a compiler to compile an instruction for execution is in the Trimberger'564's system.

As to claim 19, Trimberger'564 also discloses: executing the second instruction and the configuration further comprises retrieving operands (referred to by R1, R2, and R3 in the instruction 113, see Fig. 1) requested by the second instruction and the configuration.

As to claim 20, Trimberger'564 also discloses: the second instruction provides the operands (referred to by R1, R2, and R3 in the instruction 113, see Fig. 1) to the configuration.

As to claim 21, Trimberger'564 also discloses: a register (register R1, R2, or R3 indicated in the instruction 113, see Fig. 1) provides the operands (referred to by R1, R2, and R3 in the instruction 113, see Fig. 1) to the configuration.

As to claim 22, Trimberger'564 also discloses: the second instruction includes an immediate value field (see Col. 5, lines 28-30 regarding the immediate data from the instruction word),

the second instruction being executed with values stored in the immediate value field.

As to claim 23, Trimberger'564 also discloses: the second instruction includes an immediate value field (see Col. 5, lines 28-30 regarding the immediate data from the instruction word), the configuration being executed with values stored in the immediate value field.

As to claim 24, Trimberger'564 also discloses: decoding (by sequencer 111, see Fig. 1, and see also Col. 5, lines 23-27) controls from the second instruction (113, see Fig. 1) and the configuration; and processing data according to the decoded controls with one or more execution units (inside the CPU in the Trimberger'564's system) in parallel.

As to claim 25, Trimberger'564 also discloses: generating (by such as ALU inside the CPU in the Trimberger'564's system) one or more results with the one or more execution units (inside the CPU in the Trimberger'564's system).

As to claim 26, Trimberger'564 also discloses: writing the one or more results to a register (such as general-purpose register, Accumulator, MBR or MAR inside the CPU in the Trimberger'564's system).

As to claim 27, Trimberger'564 also discloses: storing the one or more results to a memory (such as the main memory inside the CPU in the Trimberger'564's system).

As to claim 28, Trimberger'564 also discloses: providing the one or more results to respective execution units (inside the CPU in the Trimberger'564's system). Note the ALU inside the CPU in the Trimberger'564's system needs one or more results from such as an Accumulator for obtaining a final result of an arithmetic operation.

As to claim 29, Trimberger'564 also discloses: further comprising pre-loading a second configuration register (one of the 101a-101n registers, see Fig. 1) with a configuration (CONFIG WORD 0-n, see Fig. 1) while the configuration previously loaded in the first configuration register (one of the 101a-101n registers, see Fig. 1) executes (see Col. 7, lines 1-9).

As to claim 30, Trimberger'564 also discloses: stalling the second instruction (113, see Fig. 1) while the referenced configuration register (one of the 101a-101n registers, see Fig. 1) is being loaded with a configuration (see Col. 7, lines 1-9).

As to claim 31, Trimberger'564 also discloses: the first ins (the instruction for initialize the values in configuration registers (101a-101n, see Fig. 1), see Col. 6, lines 47-50, regarding the instructions for the selected configuration word

being stored in the configuration store 101), the second instruction (113, see Fig. 1), and the configuration (CONFIG WORD 0-n, see Fig. 1) are executed as part of an application program (stored in instruction memory 110, see Fig. 1).

As to claim 32, Trimberger'564 also discloses: executing the second instruction and the configuration includes performing an operation (indicated in OPCODE 123 of instruction 113, see Fig. 1) on scalar data (note this is the situation when the operands are scalar data).

As to claim 33, Trimberger'564 also discloses: executing the second instruction and the configuration includes performing an operation (indicated in OPCODE 123 of instruction 113, see Fig. 1) on vector data (note this is the situation when the operands are used in a vector operation).

As to claim 33, Trimberger'564 also discloses: executing the second instruction and the configuration includes performing an operation on scalar data and performing an operation on vector data (note this is the situation when the operands comprise scalar data and the partial operands are used in a vector operation).

Referring to claim 36, Trimberger'564 discloses, as claimed, a processing system (see Fig. 1), comprising: means for executing (by the CPU of Trimberger'564's system) a first

instruction (the instruction for initialize the values in configuration registers (101a-101n, see Fig. 1), see Col. 6, lines 47-50, regarding the instructions for the selected configuration word being stored in the configuration store 101) that loads a configuration (CONFIG WORD 0-n, see Fig. 1) into a configuration register (101a-101n registers, see Fig. 1); and means for executing (by the CPU of Trimberger'564's system) a second instruction (113, see Fig. 1) and the configuration (CONFIG WORD 0-n, see Fig. 1), the second instruction (113, see Fig. 1) referencing (by CONFIG(X) 124, see Fig. 1) the configuration register (101a-101n registers, see Fig. 1) containing the configuration (CONFIG WORD 0-n, see Fig. 1).

Allowable Subject Matter

4. Claims 84-97 are allowed.

5. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an examiner's statement of reasons for allowance: Trimberger'564, the closest reference discloses executing a first instruction that loads a configuration into a

configuration register; and executing a second instruction and a configuration stored in a configuration register referenced by the second instruction. However, Trimberger'564 and the other cited prior art, do not teach or fairly suggest: a vector address unit providing an address to the vector register which stores the first vector elements selected by the second instruction and the configuration in combination with all of the other limitations in claim 84. Further, the combination is not obvious.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wilkinson et al.'528 discloses: SIMD/MIMD array processor with vector processing comprising a configuration register in the external memory interface as shown in Fig. 1B. Casselman'980 discloses: FPGA virtual computer for executing a sequence of program instructions by successively reconfiguring a group of FPGA in response to those instructions. An array of FPGAs change their configurations successively during performance of successive user-defined algorithms. The array includes a processor-like device capable of performing the computations necessary to

reconfigure the FPGAs in the array in accordance with the next algorithm to be performed. Greenbaum et al.'642 discloses: Compiling system and method for reconfigurable computing. A compiling system and method for generating a sequence of program instructions for use in a dynamically reconfigurable processing unit having an internal hardware organization that is selectively changeable among a plurality of hardware architectures, each hardware architecture executing instructions from a corresponding instruction set. Object files optionally encapsulate bitstreams specifying hardware architectures corresponding to instruction set architectures with executable code for execution on the architectures.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the

status of this application or proceeding should be directed to **the TC central telephone number, (571) 272-2100.**

9. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly **into the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

November 14, 2004